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Claims

[c1] A method of forming a thermistor, comprising:
forming an isolation region in a substrate including at least an upper layer of single crystal semiconductor;
depositing a salicide precursor over said isolation region and said upper layer of single crystal semiconductor;
reacting said salicide precursor with said upper layer to form a salicide self-aligned to said upper layer; and
removing an unreacted portion of said salicide precursor while preserving a portion of said salicide precursor over said isolation region as a body of said thermistor.

[c2] The method of claim 1 further comprising:
forming a layer of interlevel dielectric (ILD) over said body of said thermistor; and
forming conductive contacts to said body of said thermistor insulated by said ILD.

[c3] The method of claim 2 wherein said salicide precursor consists essentially of at least one metal selected from the group consisting of: Pt, Cu, Co, Ni, W, and Ti.

[c4] The method of claim 2 wherein said body of said thermistor has a thickness between 5 and 100 nm.

[c5] The method of claim 2 wherein said interlevel dielectric includes borophosphosilicate glass (BPSG).

[c6] The method of claim 2 wherein said single-crystal semiconductor consists essentially of silicon and said substrate is a silicon-on-insulator substrate having a buried oxide layer between said upper layer of single-crystal silicon and a bulk layer of single-crystal silicon.

[c7] The method of claim 7, wherein said isolation region is a trench isolation region.

[c8] The method of claim 1, wherein said salicide precursor is removed in a manner such that said thermistor body only overlies an isolation region.

[c9] The method of claim 9, wherein said isolation region is a trench isolation region.

[c10] The method of claim 9, wherein said isolation region is a trench isolation region.

[c11] The method of claim 1 wherein said salicide precursor is deposited over said isolation region and said upper layer of single crystal semiconductor by sputtering.

[c12] The method of claim 2 further comprising interconnecting first and second conductive patterns to respective

ones of said contacts such that said thermistor provides local interconnection between said first and second conductive patterns.

[c13] An integrated method of forming a thermistor, comprising:
forming an interlevel dielectric layer (ILD) above a first wiring level of an integrated circuit;
forming an embossed area in said ILD;
depositing a thermistor material in said embossed area and over said ILD;
patterning said thermistor material;
etching said ILD selective to said patterned thermistor material to define openings in said ILD above said first wiring level, said thermistor material serving as a hard-mask during said etching;
forming a second wiring level in said openings;
removing said thermistor material from a surface of said ILD while permitting said thermistor material to remain in said embossed area; and
forming contacts to said thermistor material.

[c14] The method of claim 14 wherein said step of forming said contacts to said remaining thermistor material includes forming a second interlevel dielectric (second ILD) above said thermistor material, forming openings in said second ILD and filling said openings with a conductor.

[c15] The method of claim 14 wherein said step of forming said contacts further includes forming an insulative capping layer above said remaining thermistor material prior to forming said second ILD and extending said openings through said insulative capping layer.

[c16] The method of claim 14 wherein said step of forming said second wiring level in said openings includes forming a conductive liner in said openings and thereafter depositing a conductor in said lined openings.

[c17] The method of claim 17 wherein said thermistor material is selected from the group consisting of organic polymeric materials such as various anti-reflective coatings (ARCs) used in semiconductor processing, inorganic materials such as silicon oxides, silicon nitrides, silicon oxynitrides and SiC, or any metallic or semi-conducting material in an amorphous, poly-crystalline, or single-crystal form.

[c18] The method of claim 14 further comprising interconnecting first and second conductive patterns to respective ones of said contacts such that said thermistor provides local interconnection between said first and second conductive patterns.

[c19] An integrated circuit thermistor, comprising:

a region of thermistor material formed in an embossed region of an interlevel dielectric (ILD); and
contacts to said thermistor material.

[c20] The integrated circuit thermistor of claim 20 wherein said ILD is a second ILD formed above a first ILD in which a first wiring level is formed.

[c21] The integrated circuit thermistor of claim 20 wherein said thermistor material is selected from the group consisting of organic polymeric materials such as various anti-reflective coatings (ARCs) used in semiconductor processing, inorganic materials such as silicon oxides, silicon nitrides, silicon oxynitrides and SiC, or any metallic or semi-conducting material in an amorphous, polycrystalline, or single-crystal form.

[c22] The integrated circuit thermistor of claim 20 wherein said contacts are connected to respective conductive patterns such that said thermistor provides local interconnection between said respective conductive patterns.